SGS-THOMSON MICROELECTRONICS

ST14C02C

CMOS SERIAL ACCESS 2K (256 x 8) EEPROM

- 1.000.000 ERASE/WRITE CYCLES MINIMUM
- OVER 10 YEARS DATA RETENTION
- SINGLE 3V to 5.5V POWER SUPPLY
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (UP TO 4 BYTES)
- PAGE WRITE (UP TO 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES

Figure 1 Delivery forms

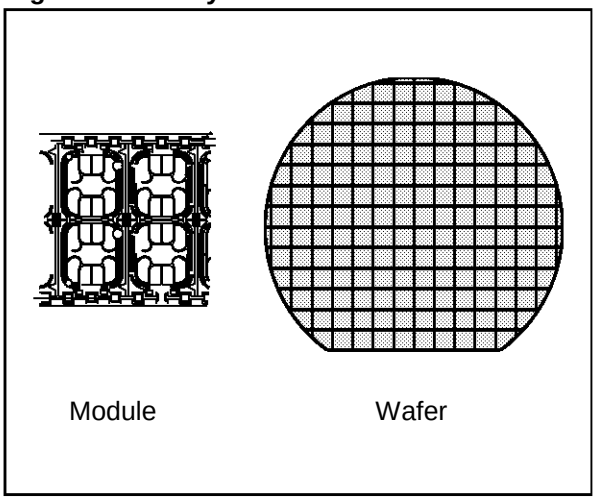
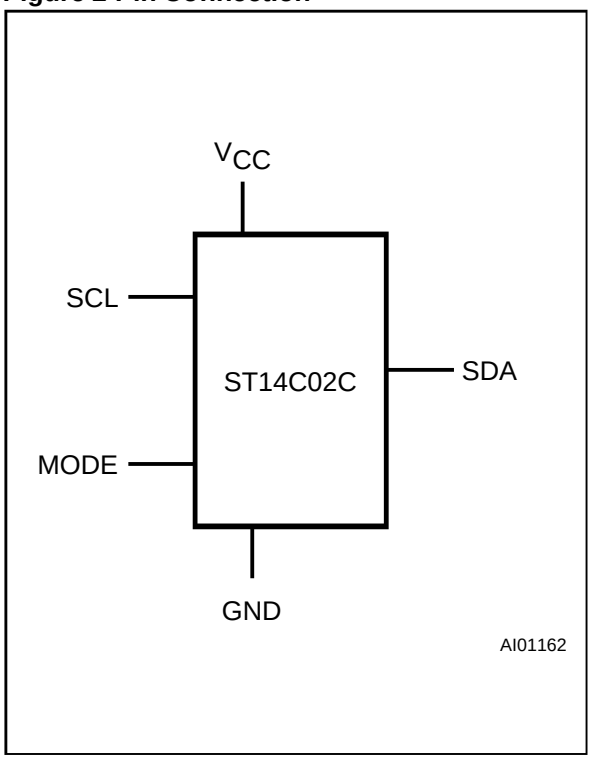


Figure 2 Pin Connection



DESCRIPTION

The ST14C02C is a 2K bit electrically erasable programmable memory (EEPROM), organized as 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which confirms an endurance of more than 1.000.000 erase/write cycles with a data retention of over 10 years. This memory operates with a supply voltage value as low as 3V.

Table 1 Signal Names

SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
GND	Ground

Figure 3 Contact Connections

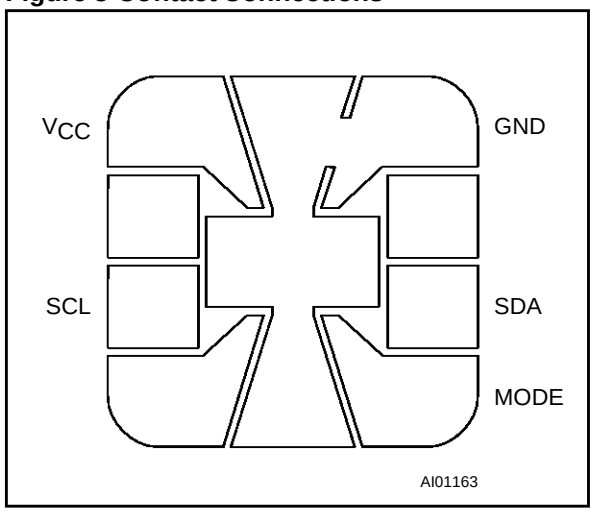
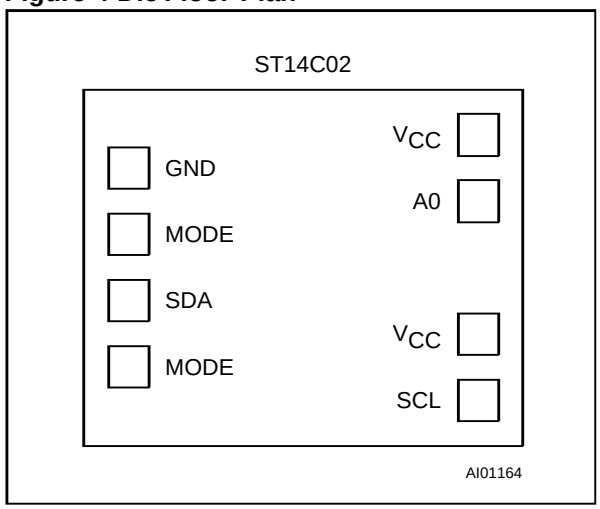


Figure 4 Die Floor Plan



Note : A0 is internally connected to GND. The two MODE pads and the two V_{CC} pads are internally connected together

Both wafers (sawn or unsawn) and micromodules (on film) are available.

The memory is compatible with the I^2C standard, two wire, serial interface which uses a bi-directional data bus and serial clock.

It carries a built-in 7 bit, unique device identification code (1010000) corresponding to the I^2C bus definition. Only one memory can be attached to the I^2C bus. This memory behaves as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010000), plus one read/write bit and terminated by an acknowledge bit.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect.

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

Table 2 Endurance and Data Retention

Device	Endurance E/W Cycles	Data Retention Years
ST14C02C	1,000,000	10

1 SIGNAL DESCRIPTIONS

1.1 Serial Clock (SCL)

The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up.

1.2 Serial Data (SDA)

The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up.

1.3 Mode (MODE)

The MODE input may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode). Note that the voltages are CMOS levels, not TTL compatible.

Table 3 Device Select Code

	Device Code							$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	0	0	0	$R\overline{W}$

Note : The MSB b7 is sent first.

Table 4 Operating Mode

Mode	$R\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, $R\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 256	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, $R\overline{W}$ = '0'
Multibyte Write	'0'	V_{IH}	4	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, $R\overline{W}$ = '0'

Note : X = V_{IH} or V_{IL}

2 DEVICE OPERATION

2.1 I²C Bus Background

The ST14C02C supports the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. This memory is always slave device in all communications.

2.2 Start Condition

START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the memory continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

2.3 Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

2.4 Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

2.5 Data Input

During data input the ST14C02C samples the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Figure 5 Maximum R_L Value versus Bus Capitance (C_{BUS}) for an I²C Bus

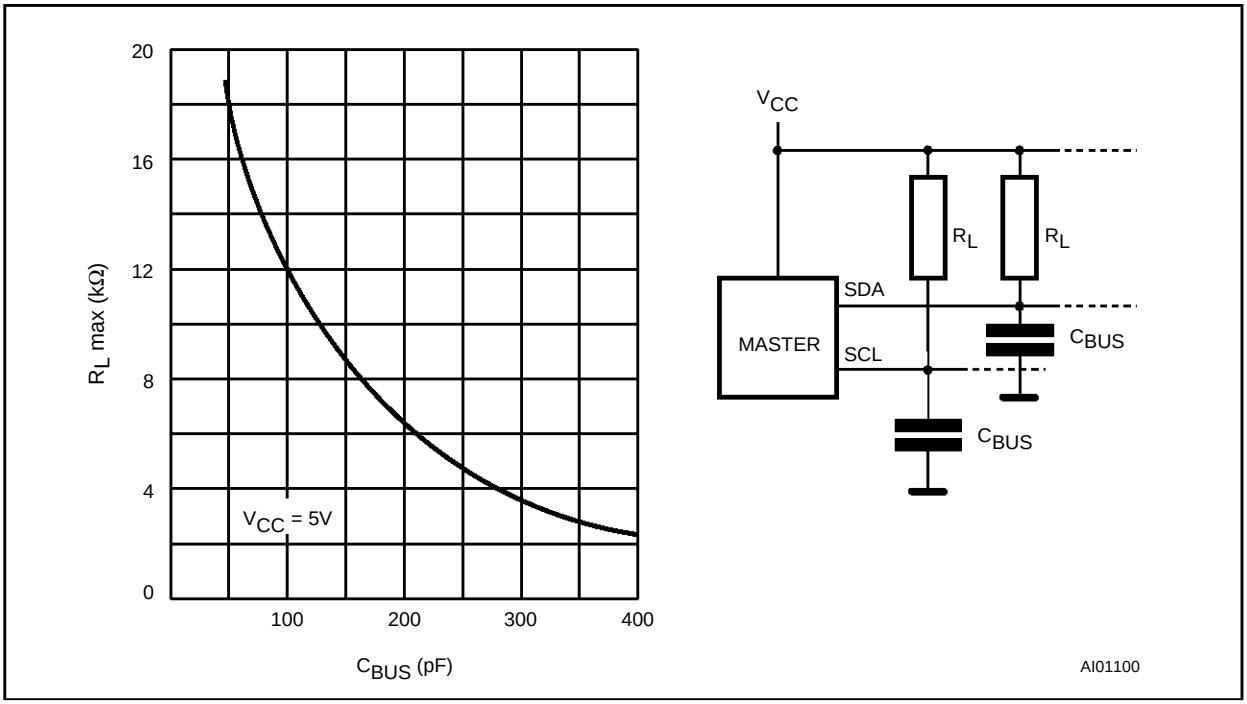


Table 5 Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature Wafer form Module form	-65 to 150 -40 to 120	°C
V_{IO}	Input or Output range	-0.3 to 6.5	V
V_{CC}	Supply Voltage	-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)	4000	V
	Electrostatic Discharge Voltage (Machine model) (3)	500	V

Notes :

1) Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2) MIL-STD-883C, 3015.7 (100pF, 1500 Ω)
3) EIAJ IC-121 (Condition C) (200pF, 0 Ω)

Table 6 DC Characteristics (T_A = 0 to 70 °C ; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		± 2	µA
I_{LI}	Input Leakage Current (MODE pad)	$0V \le V_{IN} \le V_{CC}$		± 10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC,}$ SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_c = 100kHz (Rise/Fall time < 10ns)		2	mA
I_{CC1}	Supply Currrent (Standby)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
V_{IL}	Input Low Voltage (SCL, SDA)		- 0.3	0.3 V_{CC}	V
V_{IH}	Input HighVoltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (MODE)		- 0.3	0.5	V
V_{IH}	Input High Voltage (MODE)		V_{CC} - 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 6 AC Testing Input/ Output Waveforms

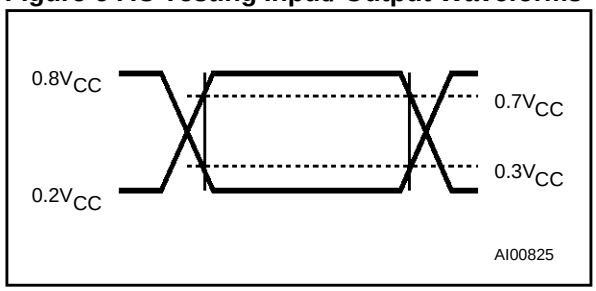


Table 7 Capacitance (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF

Note : Sampled only, not 100% tested

Table 8 AC Characteristics (T_A = 0 to 70 °C ; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL2}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_{NS}	T_I	Noise suppression Time Constant (SCL & SDA Inputs)		100	ns
t_W (2)	t_{WR}	Write Time		10	ms

Notes 1) For a reSTART condition, or following a write cycle.
2) In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms

2.6 Memory Addressing

To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

The 7 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 7 bits are fixed as 1010000b (A0h).

The 8th bit sent is the read or write bit ($\overline{RW}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

2.7 Write Operations

The Multibyte Write mode is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

2.8 Byte Write

In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

2.9 Multibyte Write

For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 6 most significant address bits A7-A2), the programming time is then doubled to a maximum of 20ms.

Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes only if the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same 'row'.

When not connected, the MODE pin is internally pulled up to "1" and the multibyte write option is selected.

2.10 Page Write

For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

2.11 Minimizing System Delays by Polling On ACK

During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master.

The sequence is as follows:

- Initial condition: a Write is in progress.
- Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

2.12 Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all “1’s” (or FFh).

2.13 Current Address Read

The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the RW bit set to ‘1’. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

2.14 Random Address Read

A dummy write is performed to load the address into the address counter, see Figure 11. This is followed by another START condition from the master and the byte address is repeated with the R/W bit set to ‘1’. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

2.15 Sequential Read

This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will ‘roll- over’ and the memory will continue to output data.

2.16 Acknowledge in Read Mode

In all read modes the memory waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST14C02C terminates the data transfer and switches to a standby state.

Figure 7 Read Modes Sequence

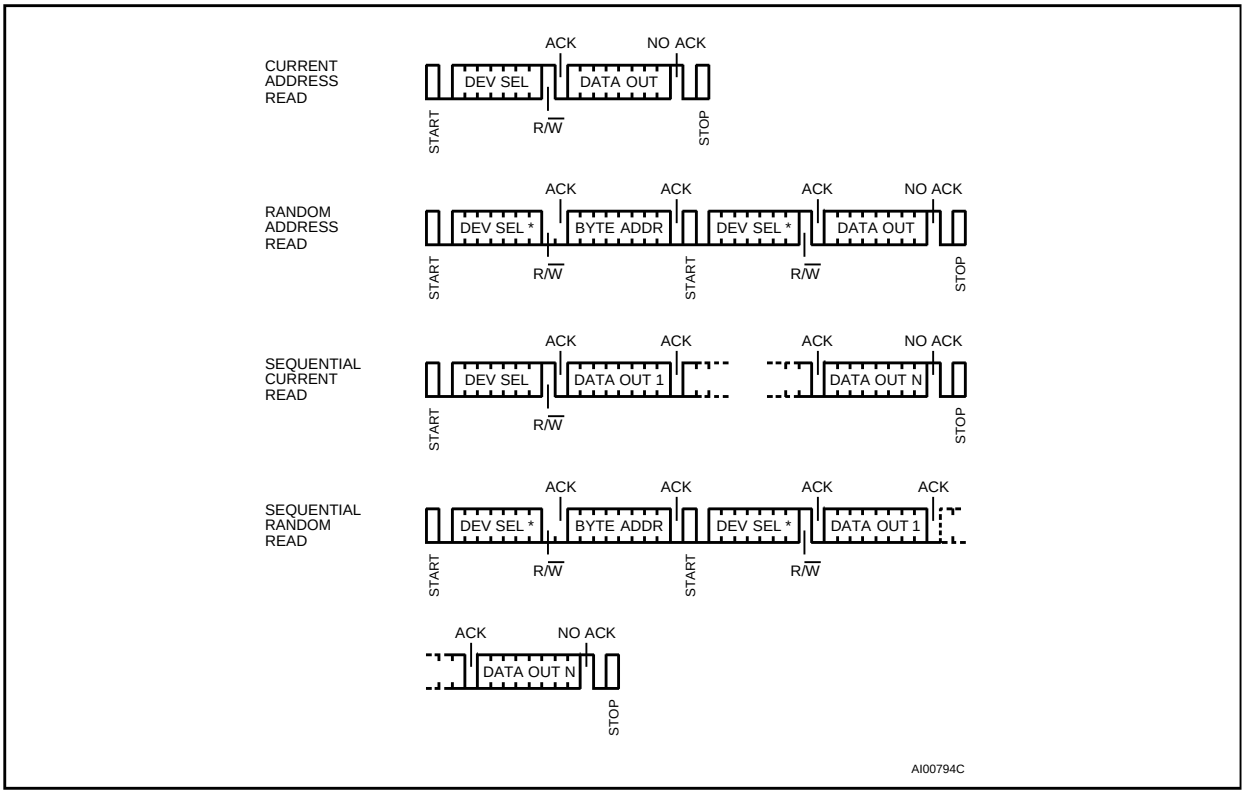


Figure 8 AC Waveforms

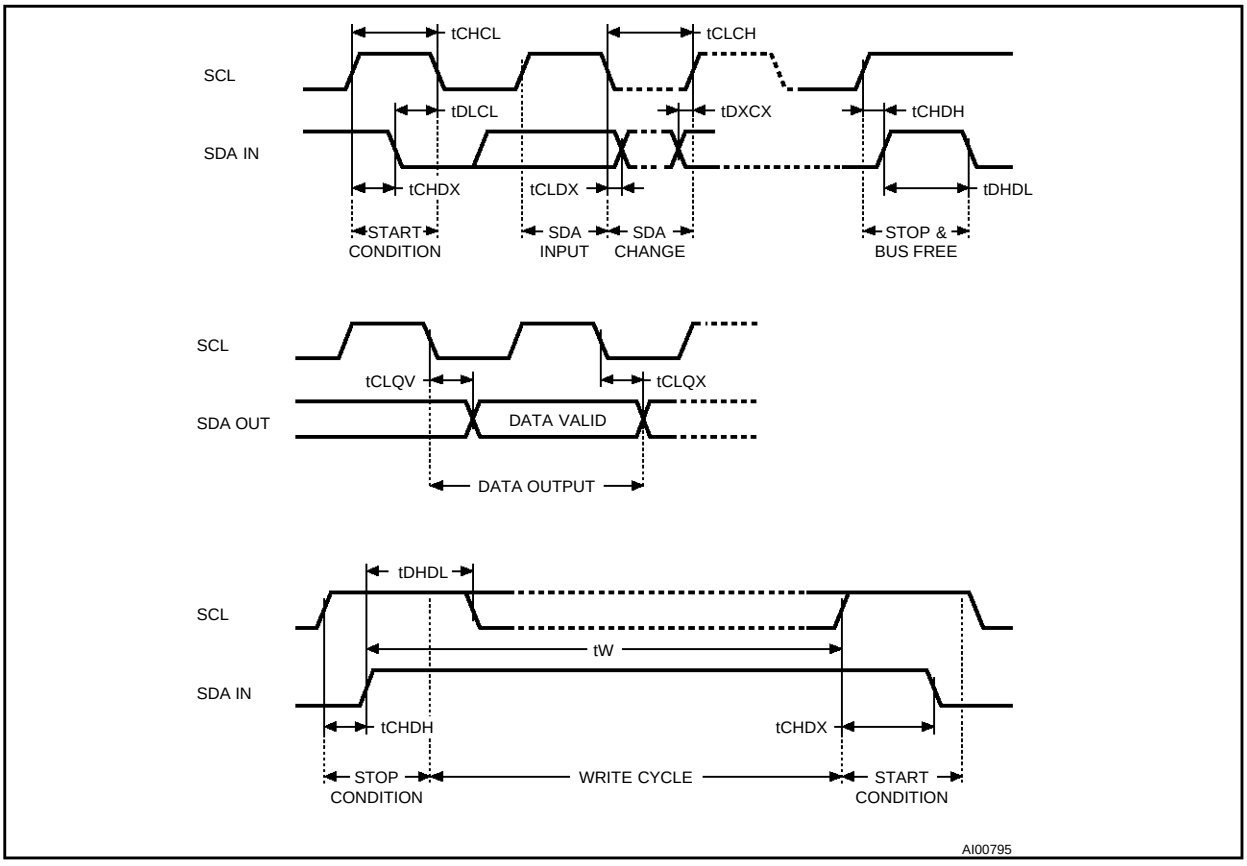


Figure 9 I²C Bus Protocol

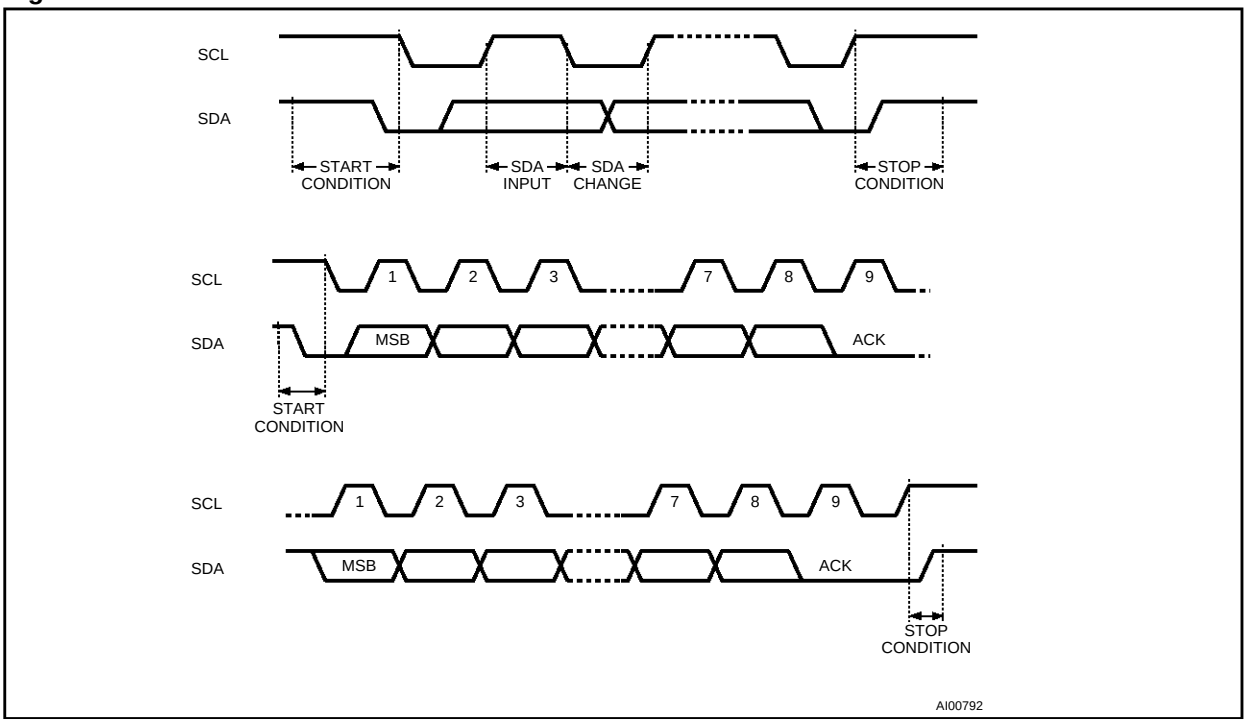


Figure 10 Write Cycle Polling using ACK

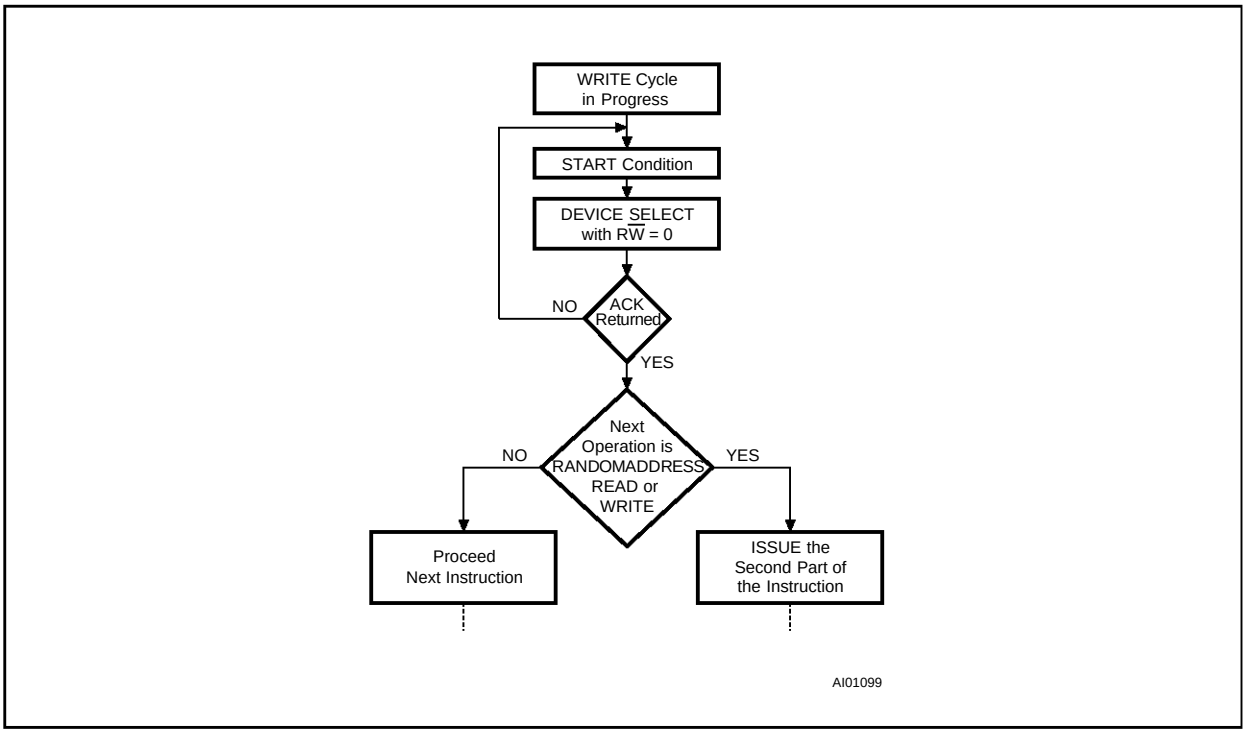
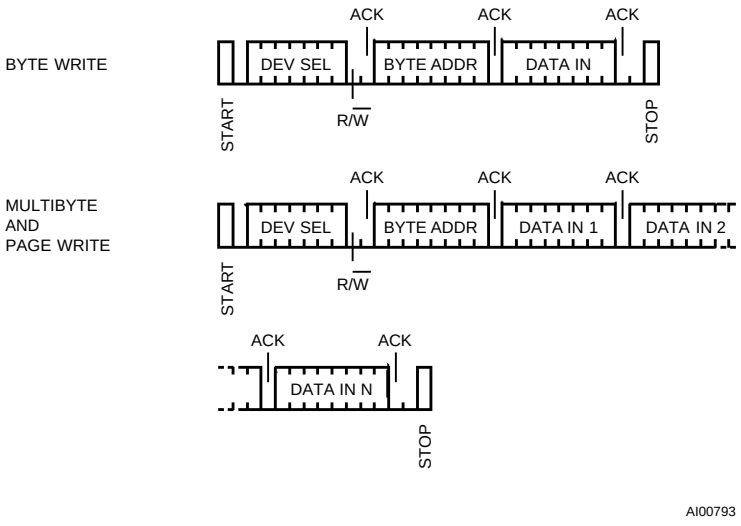


Figure 11 Write Modes Sequence



3 ORDERING INFORMATION

3.1 Sales Types Available

SAWN WAFER	UNSAWN WAFER	MODULES
ST14C02CS21	ST14C02CW2	ST14C02CD20
ST14C02CS22	ST14C02CW4	
ST14C02CS23		
ST14C02CS24		
ST14C02CS41		
ST14C02CS42		
ST14C02CS43		
ST14C02CS44		

Note :

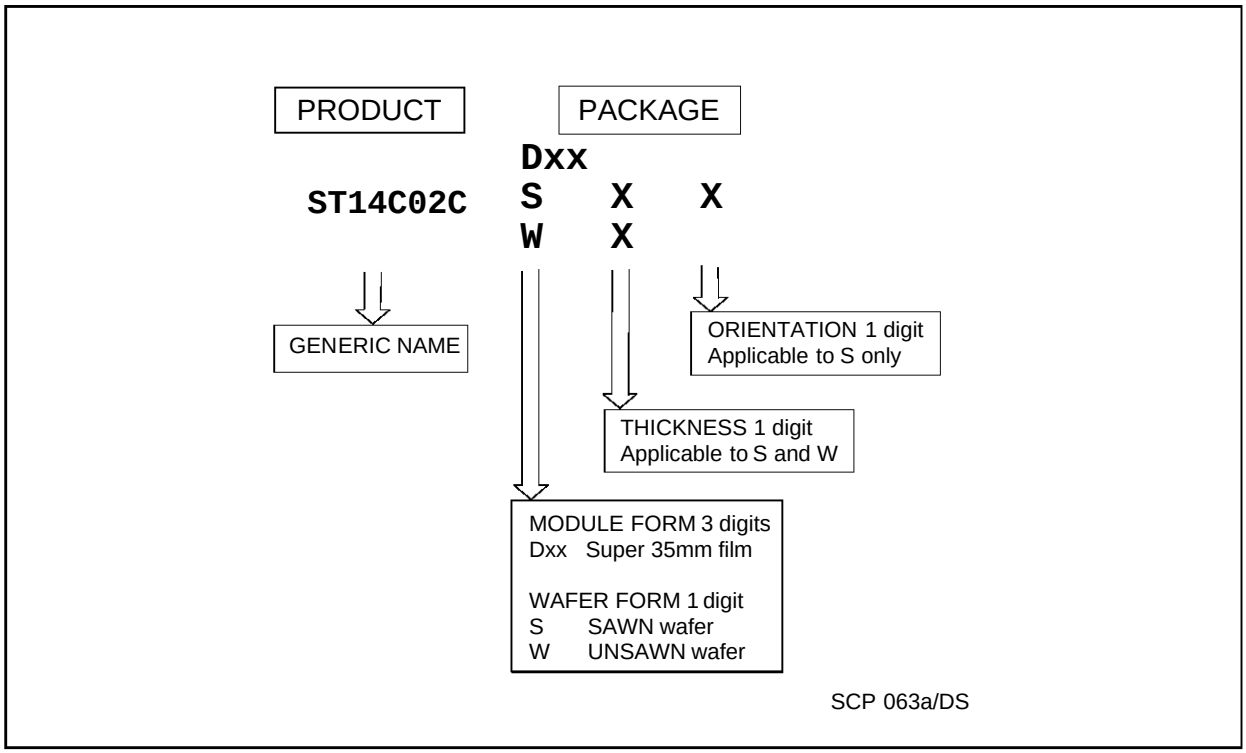
– Parts are shipped with the memory content set at all “1’s” (FFh).

– For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

3.2 Wafer Thickness

THICKNESS	UNSAWN	SAWN
275µm ± 25µm	W2	S2
180µm ± 15µm	W4	S4

Figure 12 Sales Types Architecture



3.3 Sawing Orientation

Sawn wafers are scribed and mounted on adhesive tape into a frame. The orientation of the die with respect to the plastic frame notches has to be specified by the Customer.

The orientation is defined by the position of the GND pad of the die versus the notches of the frame, active area of product visible.

Caution : Wafers mounted on adhesive tape must be used within a limited period after the mounting date :

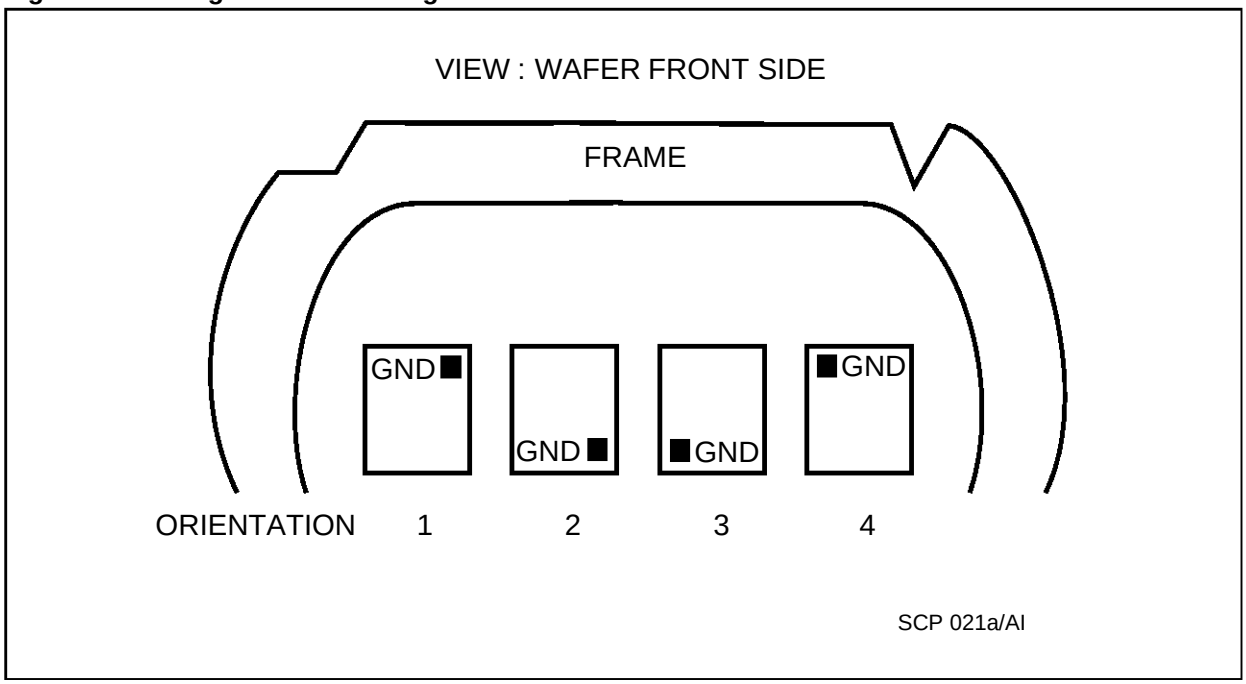
– 2 months,
if wafers stored at 25°C, 55% Relative Humidity

– 6 months,
if wafers stored at 4°C, 55% Relative Humidity

Table 9 Sawing Orientation Coding

ORIENTATION	CODE
GND top right	1
GND bottom right	2
GND bottom left	3
GND top left	4

Figure 13 Sawing Orientation Diagram



.